Paper No. 37

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

_____

Ex parte TERRY G. RITZ

_____

Appeal No. 1996-3541
Application 08/275,307

_____

ON BRIEF

_____

Before THOMAS, FLEMING and BARRY, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

The above-captioned panel only recently received again this appeal for decision following the remand to the examiner on November 9, 1999. Pending appealed claims remain as 1 through 21 and 23 through 35, which constitute all the claims in the application.

Representative claim 1 is reproduced below:

1. In a microcontroller of the type which includes an execution unit for executing stored program instructions, a memory system for storing said program instructions and comprising:

memory means for storing said program instructions, said memory means including a static random access memory; and

program interface means coupled to said static random access memory and arranged to be coupled to an external source of said program instructions for providing said static random access memory with said program instructions from said external source of said program instructions for use by said microcontroller to control a device as a device driver.

The following references are relied on by the examiner:

Goodman et al. (Goodman)	4,099,236	July 4, 1978
Andersen et al. (Andersen)	4,718,003	Jan. 5, 1988

Claims 30 through 34 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Goodman. All claims on appeal, claims 1 through 21 and 23 through 35, stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon Andersen alone. The supplemental examiner's answer issued in response to the earlier-noted remand order from this panel does not affirmatively state that the other rejections of record from the final rejection have been formally withdrawn. Since they have not been repeated in the latest answer, we consider them to have been withdrawn by the examiner in response to the remand order. Appellant's most recent reply brief in response to this latest answer implicitly agrees.

Rather than repeat the positions of the appellant and the examiner, reference is made to all of the various briefs and reply briefs as well as answers and supplemental answers filed in this appeal.

OPINION

We reverse both art rejections of record and institute two new rejections, one under the first paragraph of 35 U.S.C. § 112 and another under 35 U.S.C. § 103 interpreting the Andersen reference in a different manner than the examiner.

Turning first to the rejection of claims 30 through 34 under 35 U.S.C. § 102 as anticipated by Goodman, each of independent claims 30 and 33 require that a master microprocessor essentially program a memory by causing instructions to be stored therein. Master processor 11 in Figure 1 of Goodman is not taught to perform this function either in the RAM 10 or any other memory element that may be associated with the DMA controller 12 and/or the slave processor 13. Although the RAM 10 is taught to be either a dynamic or static RAM, it too is not disclosed to store instructions for any of the processing devices 11 through 13. Even though the bidirectional bus 14 conveys data bidirectionally among the devices in Figure 1, none of the data are taught to comprise instruction or programming-type information. The slave processor 13 contains its own ROM as pointed out by appellant which, on its own, would not be given to being programmed or reprogrammed, once it has been initially programmed, by any

of the other devices 11 and 12. As indicated at the bottom of column 2, this ROM stores programs only for the slave processor 13. Therefore, we reverse the rejection of claims 30 through 34.

We also reverse the rejection of each independent claim on appeal and, as a consequence, each of the dependent claims so rejected under 35 U.S.C. § 103 over Andersen alone. As appellant brings out in the various briefs, the program memory 26 provides stored programs for the microcomputer 22 and not for the programmable controller 12. Because this program memory 26 is taught at column 3, lines 21 and 22 to be a PROM, the examiner's view that this obviously may be comprised of a SRAM is misplaced because they represent different structural approaches to storing information. Moreover, the key feature required of the claims that some external computer or device program or reprogram the memory 26 as alleged by the examiner, is not met by Andersen since it fails to teach this feature in any manner relative to the positions argued by the examiner. The personal computer 10 in Andersen is not taught to program or reprogram memory 26. Thus, the rejection of claims 1 through 21 and 23 through 35 as being obvious over Andersen alone is reversed.

REJECTIONS UNDER 37 CFR § 1.196(b)

Claims 30 through 35 are rejected under a written description portion of 35 U.S.C. § 112, first paragraph. These claims were new claims entered by amendment on May 15, 1995. Because the programmability feature of independent claims 30 and 33 is stated in the claims to relate to microinstructions, and because the original filed specification, drawings and original claims do not indicate programmability of the static RAM 14 at the level of microinstructions, the rejection of claims 30 through 35 is appropriate. There is no evidence of record in the application papers filed according to the filing date of appellant contemplating the use of microinstructions as a type of instruction that is programmed into static RAM 14 according to the general teachings of the specification and requirements of the claims.

Claims 1, 11, 23, 24, 25, 28 through 33 and 35 are rejected under 35 U.S.C. § 103 as being obvious over Andersen alone. The teachings at column 1, lines 29 through 38 and column 2, lines 27 through 48 indicate first that the programmable controller 12 in Figure 1 controls an apparatus and/or process related thereto to the extent this feature is recited in any of the listed claims. More importantly, however, these noted portions of columns 1 and 2 indicate that another computer, such as personal computer 10, provides programming of the programmable controller 12 itself. For this to occur, we find that the structure within the programmable controller 12

would have been prima facie in the form of a static RAM since such were well-known in the art well before the filing date of appellant's application. Such programmable controllers were also well-known to encompass their own execution units for executing ladder diagram sequencing operations to control specific devices. In accordance with Andersen's teachings and showings, the integrated circuit element 14 comprises the claimed programming and/or interface means between the personal computer 10 and the programmable controller 12. Since the computer 10 is specifically identified as comprising a personal computer, it obviously would have been embodied in the form of a microprocessor as set forth, for example, in dependent claim 24. Appellant's own specification at page 8, lines 2 and 3 indicates that the static random access memory 14 that he utilized is well-known in the art. As such, such devices are well-known not to retain information stored therein when operating power is removed as recited in dependent claims 31 and 32. To complement this rejection, the examiner is expected to consider the programmable controller art in class 700 beginning at subclass 11 in considering any additional rejections to the dependent claims as well as embellishing upon this rejection we have made.

SUMMARY

In summary, we have reversed the rejection of claims 30 through 34 under 35 U.S.C. § 102. We have also reversed the rejection of claims 1 through 21 and 23 through 35 under 35 U.S.C. § 103. We have instituted two new rejections under the provisions of 37 CFR § 1.196(b). These include a rejection of claims 30 through 35 under the written description portion of 35 U.S.C. § 112, first paragraph, and a rejection of claims 1, 11, 23, 24, 25, 28 through 33 and 35 under 35 U.S.C. § 103.

This decision contains new grounds of rejection pursuant to 37 CFR § 1.196(b)(amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)). 37 CFR § 1.196(b) provides that, "A new ground of rejection shall not be considered final for purposes of judicial review."

37 CFR § 1.196(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of proceedings (§ 1.197(c)) as to the rejected claims:

> (1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner. . . .

(2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record. . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

REVERSED
37 CFR § 1.196(b)

James D. Thomas Administrative Patent Judge	))))) BOARD OF PATENT
Michael R. Fleming Administrative Patent Judge	)) APPEALS AND)) INTERFERENCES
Lance Leonard Barry Administrative Patent Judge	))

JDT/cam

Foley & Lardner
3000 K Street, N.,W., Suite 500
P. O. Box 25696
Washington, DC 20007-8696